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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,382	12/05/2001	Louise A. Koss	10010863-1	2960

7590 10/19/2005

AGILENT TECHNOLOGIES, INC.
Legal Department, DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,382	KOSS ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Appeal Brief

In view of the ***Appeal Brief*** filed on 7/26/2005, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

This is a Non-Final Office Action in response to the ***Appeal Brief*** filed on 7/26/2005. Claims 1-8 are pending and presently under examination.

Response to Arguments

Applicant's arguments see ***Appeal Brief*** filed on 7/26/2005, with respect to the rejection of claims 1-8 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of claims 1-4 under 35 U.S.C. 102(b) as being anticipated by

Talley (U.S. Patent No. 5,301,156). Claims 5-8 are objected because pf allowable subject matter.

In response to Applicant's argument, in reference to independent claim 1, the Examiner agrees that Bhavsar does not disclose a control circuit "embedded in a control and address block of a RAM circuit". However, upon a new ground of rejection, Talley discloses a control circuit (106) embedded in a control and address block (address register 104, write register 108, and read register 110, each connected to a global bus 112) in the RAM circuit (VLSI chip).

Claims 1-4 are rejected over the prior art and claims 5-8 are objected because pf allowable subject matter, as set forth in the present Office Action, herewith.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Talley (U.S. PATENT NO: 5,301,156) ISSUED: April 5, 1994.

Regarding independent Claim 1, Talley discloses an electronic circuit [an embedded RAM (Random Access Memory) circuit 100] for self-test testing a random access memory array (RAM 102) embedded in a RAM circuit (VLSI chip), wherein

RAM 102 having a plurality of storage cells organized into a plurality of slice arrays. The Embedded RAM circuit 100 includes RAM 102, an address register 104, a control circuit 106, a write register 108, and a read register 110, wherein RAM 102 includes read and write latches, and address and control logic, in addition to the RAM memory cells, Figure 1, see Summary of the Invention and Abstract, the Embedded RAM circuit 100, comprising:

Control circuit (106) embedded in a control and address block (address register 104, write register 108, and read register 110, each connected to a global bus 112) in the RAM circuit (VLSI chip). Control circuit 106 controls address register 104, write register 108, and read register 110. Control circuit 106 is the controller for the VLSI chip and is normally a programmable logic array (PLA). Write register 108 provides data, which is to be written to RAM 102 via a write bus 109. Read register 110 accepts data from RAM 102 over a read bus 111, (see, Figure 1 and col. 3, lines 38-65).

Address generator 304, test controller 306, and data generator 308 all form a dedicated state machine, which generates test patterns and cycles RAM 102 through a predefined sequence of read/write operations. A data receptor 312 is connected to read bus 111. Data receptor 312 accepts the data produced by RAM 102 during read operations and either compares the data to expected results or stores the data for later comparison (see, Figure 3, Col. 5, lines 25-35).

An error detection circuit, such as a signature generator used to compile the test results, which receives data read from the RAM and produces a unique signature. Since each data term input to the signature generator will effect the unique test

signature, comparison with a predetermined, expected signature will indicate whether any data errors have occurred. See Summary of the Invention, Abstract and Figure 4.

Regarding Claim 2, Talley discloses the electronic circuit [embedded RAM circuit 100] is embedded within the RAM circuit (VLSI chip) integrated circuit, Figure 1.

Regarding Claim 3, Talley discloses the control circuit (106) is embedded in a control and address block (address register 104, write register 108, and read register 110, each connected to a global bus 112) in the RAM circuit (VLSI chip), Figure 1.

Regarding Claim 4, Talley discloses the control circuit 106 controls address register 104, write register 108, and read register 110. Control circuit 106 is the controller for the VLSI chip and is normally a programmable logic array (PLA). Write register 108 provides data, which is to be written to RAM 102 via a write bus 109. Read register 110 accepts data from RAM 102 over a read bus 111, (see, Figure 1 and col. 3, lines 38-65).

Allowable Subject Matter

Claims 5-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention as recited in claims 5 and 7. Claims 6 and 8 are directly depended upon claims 5 and 7, respectively, and therefore are also allowable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2133

By: _____.

Randolph Building, 401 Dulany Street,
Alexandria, VA 22314
Tel: (571) 272-3824, Fax: (571) 273-3824
james.kerveros@uspto.gov

Date: 3 October 2005
Office Action: Non-Final Rejection